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Hydrophobic Gate Dielectric Materials for Thin-Film Transistors: Advances, Challenges, and Applications

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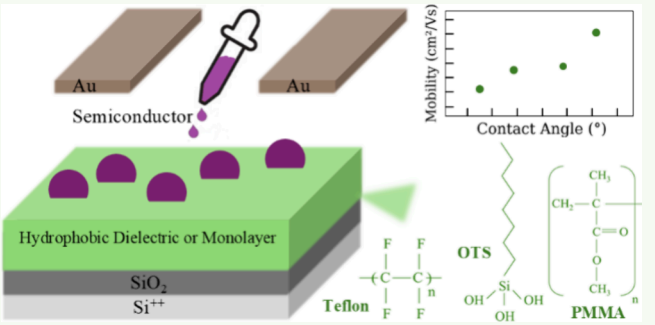
ABSTRACT: Hydrophobic gate dielectrics in thin-film transistors (TFTs) show great potential in improving device performance and stability. This is the first review that addresses this topic, summarizing existing knowledge complemented by analysis of reported findings to explore the role of hydrophobic materials as gate dielectrics in advancing organic, inorganic and solution-processed TFT technologies. Hydrophobic gate dielectrics in TFTs offer multiple advantages, including reduced charge trapping and preventing moisture absorption. These properties lead to enhanced carrier mobility, lower hysteresis, more stable threshold voltages, and long-term performance. Additionally, these materials are compatible with scalable and cost-effective deposition techniques like spin coating, chemical vapor deposition (CVD), and printing, making them ideal for large-scale electronics manufacturing. This review provides a comprehensive account of the theoretical foundations, experimental findings, and prospects of hydrophobic dielectrics in TFT applications, highlighting their pivotal role in advancing next-generation technologies.



KEYWORDS: *Thin-Film Transistors, Gate Dielectric, Hydrophobicity, Surface Energy, Fluoropolymers, Inorganic High-k Dielectrics, Polymer Dielectrics, Self-Assembled Monolayers*

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1. INTRODUCTION

Thin-film transistors (TFTs) are important parts of modern electronic systems. They act as switches or amplifiers to control electrical signals. TFTs are essential for displays, sensors, and flexible electronics.[1−3] Structurally, a TFT comprises a semiconductor layer, a gate dielectric, and electrodes (source, drain, and gate), all deposited on a substrate. The gate dielectric is a critical insulating layer that separates the gate electrode from the semiconductor, preventing current leakage and enabling field-effect control of the semiconductor channel. Its properties such as dielectric constant and thickness significantly impact device performance, influencing parameters like operating voltage, transconductance, and carrier mobility. Common dielectric materials include silicon dioxide (SiO_2),[4,5] aluminum oxide (Al_2O_3),[6,7] and organic polymers such as poly(methyl methacrylate) (PMMA)[8−10] and CYTOP.[11,12]

Hydrophobic materials are characterized by their ability to repel water and other polar molecules. This property is the result of their low surface energy, and it is often quantified by the contact angle of a water droplet on its surface. By reducing moisture absorption and charge trapping, they lead to better carrier mobility, stable threshold voltage, and longer device life.[13,14] Examples are fluorinated polymers, self-assembled monolayers (SAMs), and hybrid organic−inorganic materials.[15−18] Surfaces can be categorized into three main groups: highly hydrophobic with water contact angles above 90°, often exceeding 150° for superhydrophobicity, moderately hydrophobic with intermediate contact angles (around 90°), and hydrophilic with contact angles below 90°. It is worth noting that while water is commonly used as the reference liquid, characterizing wettability often requires testing with solvents of the materials being deposited. In that case, the term "non-wettable" more accurately reflects the surface behavior. We will use the term "hydrophobicity" as it is commonly referenced in the literature relevant to the topics discussed in this paper.[19,20]

Sometimes, gate dielectric hydrophobicity is avoided to allow for solution processing of subsequent layers. In that case, the surface of the dielectric material is treated. Examples include treating CYTOP surface using a protein solution,[12] oxygen plasma treatment of a hydrophobic poly(4-vinylphenol) (PVP) surface to print hydrophilic PEDOT ink,[21] ultraviolet-ozone (UVO) treatment of PDMS,[22] inserting a

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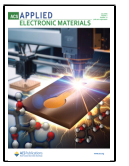

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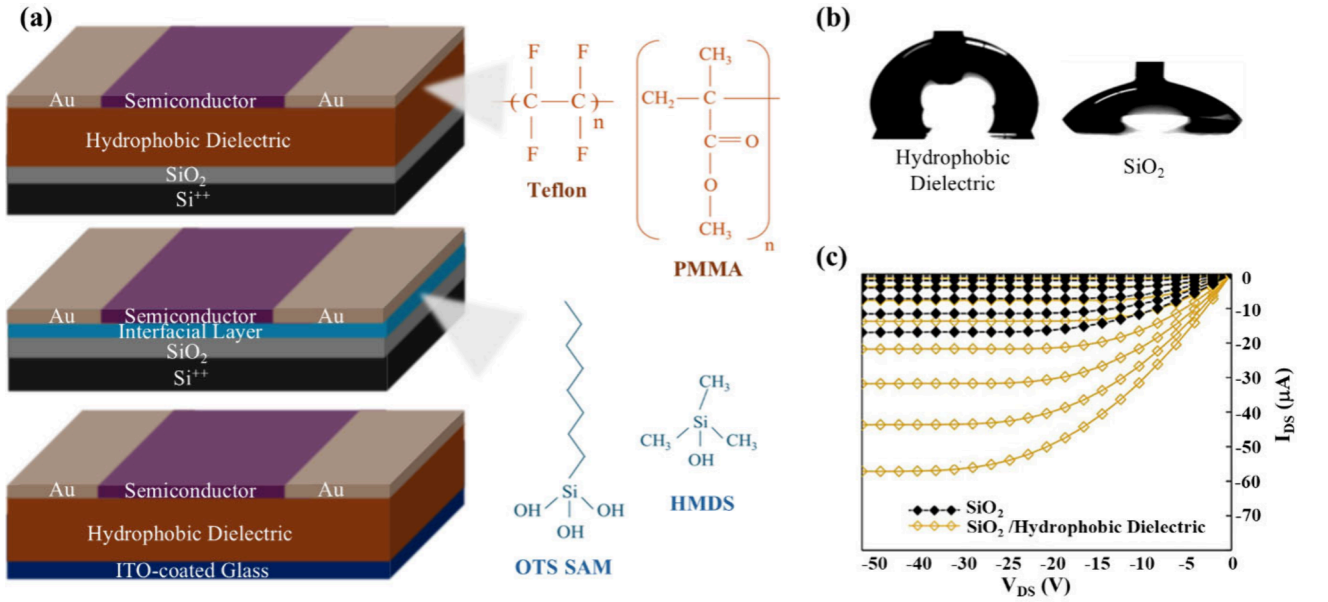

Figure 1. Hydrophobic-interface strategy for water-resistant TFTs: (a) Schematic TFT cross-section highlighting the added hydrophobic layer (in bilayer and single layer structures) with examples of polymeric dielectrics such as Teflon-AF and PMMA and interfacial layers such as HMDS and OTS SAM. (b) Images of water droplets on hydrophobic dielectrics/SAMs and SiO_2. (c) Output characteristics of an OTFT fabricated on bare SiO_2 versus the same device after inserting a hydrophobic dielectric.

ZrO_2 thin film between hydrophobic PVP surface and aqueous solutions,[23] and air plasma treatment of Teflon amorphous fluoropolymer (Teflon-AF) to inkjet-print silver nanoparticle ink.[3]

Here we aim to explore the significant benefits of hydrophobicity in TFT applications. In general, surface hydrophobicity corresponds to low surface energy, which, in turn, reduces the density of interfacial trap states between the dielectric and semiconductor layer. This trap reduction leads to improved electrical performance, minimized hysteresis (difference in current between forward and reverse voltage sweeps), and enhanced stability against bias stress.[24,25] Semiconductors such as pentacene require a hydrophobic and smooth substrate to crystallize in large grains. For example, using polytetrafluoroethylene (PTFE) (or Teflon) on SiO_2 increases the contact angle from 24.17° to 60.06° (for a 12 nm-thick layer) and reduces the surface energy from 53.54 to 32.43 mJ/m^2. Thus, improving charge transfer and operating voltage by providing a smoother surface.[26] Similarly, PMMA hydrophobicity helps with the structured growth of the organic semiconductor, leading to better sensitivity in ammonia detection in TFTs that operate as gas detecting devices.[9]

Figure 1 summarizes the central concept of this review. Using a hydrophobic dielectric or even a nanometre-thin self-assembled monolayer such as hexamethyldisilazane (HMDS) or (octadecyltrichlorosilane) OTS SAM, in a conventional SiO_2-gated OTFT, displaces interfacial water and lowers surface energy. As illustrated by the comparative output plots, this simple modification sharply increases I_{on}/I_{off} ratio. The schematic also shows typical hydrophobic layer (in bilayer and single layer structures) with examples of polymeric dielectrics such as Teflon-AF and PMMA and interfacial layers such as HMDS and OTS SAM that have been successfully integrated by solution or vapor processing, foreshadowing the deposition and performance discussions in this review.

A hydrophobic surface can be achieved with different materials and combinations. Figure 2 shows a histogram of the

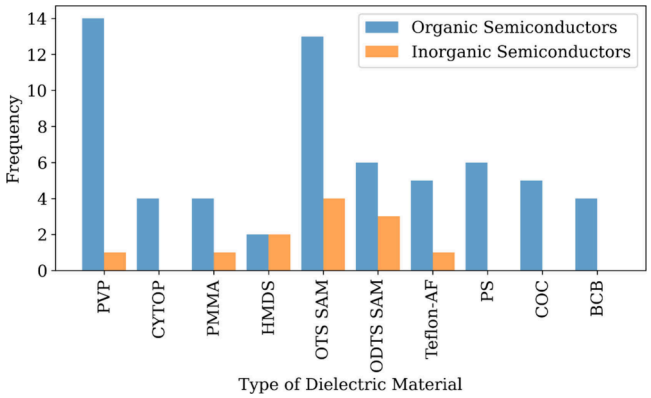

Figure 2. Histogram of top 10 hydrophobic dielectric materials in TFTs by number of literature references.

number of literature references for the 10 most common hydrophobic dielectric surfaces used in TFTs: PVP, CYTOP, PMMA, OTS SAM, HMDS, Teflon-AF, octadecyltrichlorosilane (ODTS) SAM, benzocyclobutane (BCB), polystyrene (PS), and cyclic olefin copolymer (COC).[10] These materials, the TFTs configurations incorporating them, the theories, characterization techniques, deposition methods, applications, and future research in improving device parameters will be discussed in the following sections.

This review evaluates the performance of hydrophobic dielectrics in TFTs over the past two decades, drawing from more than 100 references, supported by mathematical models that correlate dielectric properties to device performance. Additionally, it examines the processing techniques and surface treatments used to optimize hydrophobicity for various applications.

2. CATEGORIZING GATE DIELECTRICS

Gate dielectric materials used in TFTs can be categorized not only by their chemical composition but more importantly by

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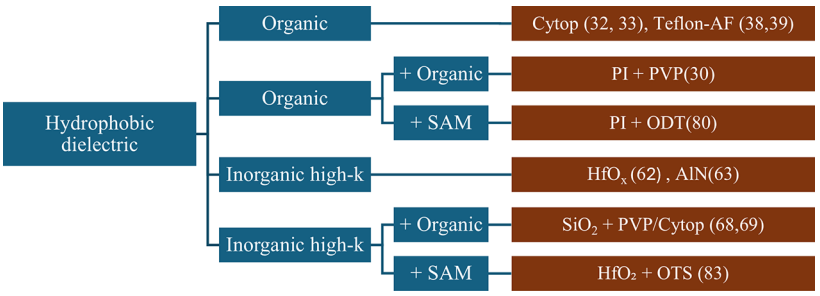

Figure 3. Different groups of dielectric materials and structures with examples given on the right.

Table 1. Common Hydrophobic Materials Used as a Gate Dielectric or Dielectric Surface Treatment Layer

Material	Material Group	Water Contact Angle (°)	Dielectric Constant	T_g (°C)	Ref.
PTFE (Teflon)	Fluoropolymer	108−112	2.0−2.1	100−120	25, 26
Teflon-AF	Amorphous fluoropolymer	107−120	1.8−1.9	160 or 240 (grade-dependent)	3, 42−44
CYTOP	Amorphous fluoropolymer	108−115	2.0−2.1	108	12, 34
PVP	Vinyl polymer	70−89	3.4−3.8	150 to 180	42, 45
PMMA	Acrylic polymer	70−100	2.6−3.0	105	4, 8, 10, 46
PS	Hydrocarbon polymer	92−98	2.6	100	4, 47
COC	Polyolefin	90−101	2.3−2.4	130	28, 48
BCB	Aromatic thermoset	85	2.7	350	49, 50
OTS	SAM	91−115	2	N/A	51−53
ODTS	SAM	73−107	2	N/A	54, 55
HMDS	Organosilane	109−110	2.3	N/A	52, 56
Parylene-C	Chlorinated parylene polymer	85−97	3.1	13−80	40, 57, 58
Parylene-F	Fluorinated parylene polymer	104−110	2.6	60−66	40, 41

their structural configuration in the device (see Figure 3). This review adopts a performance-guided classification that distinguishes materials based on their physical layering (single-layer vs bilayer) and the role they play at the dielectric/semiconductor interface. This functional framework reflects how dielectrics are selected and engineered in practice to balance trade-offs among leakage current, dielectric constant, and environmental stability. The following subsections explore organic, inorganic, and hybrid dielectric architectures, both as standalone layers and in bilayer combinations, with a focus on how structural design improves device performance. Organic and inorganic materials have been used as a single layer or in a multilayer structure (mostly bilayer). SAMs have also often been used as a top layer to provide the desired hydrophobicity at the dielectric/semiconductor interface.

2.1. Single-Layer and Bilayer Polymer Dielectrics. Polymer dielectrics are widely used due to their mechanical flexibility, solution processability, and tailorable surface properties. These characteristics make them ideal for flexible electronics, low-cost fabrication, and integration with organic semiconductors.[25,27] Single-layer polymer dielectrics provide simplicity in fabrication and offer advantages such as chemical stability, moisture resistance, and smooth surfaces that reduce charge trapping at the dielectric/semiconductor interface. For example, COC with a water contact angle of 95°, improves air stability of devices and prevents electron trapping, resulting in performance stability without hysteresis.[28] A solution-processed thin film of PMMA facilitates the structured growth of the organic semiconductor dinaphtho[2,3-*b*:2′,3′-f]thieno[3,2-*b*]thiophene (DNTT).[9] A hydrophobic fluorinated polymer patterned dielectric barrier (PDB) has been applied onto a PVP gate dielectric using transfer-printing leaving a cavity for the semiconductor deposition. This PDB significantly reduces the vertical leakage current by 2 orders of magnitude by providing selective wettability for the organic semiconductor 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS PEN).[29] Bilayer systems, on the other hand, combine the advantages of two classes of dielectric materials to optimize performance.[30] For instance, cross-linked PVP (cPVP) treated with a graftable fluorinated polymer forms a smooth and hydrophobic final top surface, reducing charge trapping, improving electrical stability, and significantly decreasing the threshold voltage shift.[31]

One group of hydrophobic dielectrics that is commonly used in the development of TFTs is fluorinated polymers. The introduction of fluorine atoms into polymer chains lowers surface energy, resulting in a highly hydrophobic dielectric surface (see Table 1). For example, CYTOP and Teflon-AF have shown contact angles exceeding 100°, which leads to reduced hysteresis and improved stability under prolonged bias stress. Moreover, the strong electronegativity of fluorine atoms leads to a reduction in charge trapping at the dielectric/semiconductor interface. This is because fluorinated surfaces have fewer hydroxyl groups, which are typically responsible for charge trapping and hysteresis in nonfluorinated dielectrics.[3,32−36]

Beyond fluorinated polymers, Parylene-based dielectrics (Parylene-C and Parylene-F) add a valuable hydrophobic option. Room-temperature chemical-vapor deposition yields pinhole-free, conformal films that act both as gate insulators and as robust encapsulants. Parylene-C has already enabled high-mobility, 3D-stacked printed logic circuits and ultralow-noise OTFTs, while fluorinated Parylene-F pairs well with solution-processable semiconductors in flexible sensor arrays and shows reversed DC-bias stress shifts that improve long-term stability.[37−41]

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Common gate dielectric materials are listed with their properties in Table 1 and their chemical structures are depicted in Figure 4.

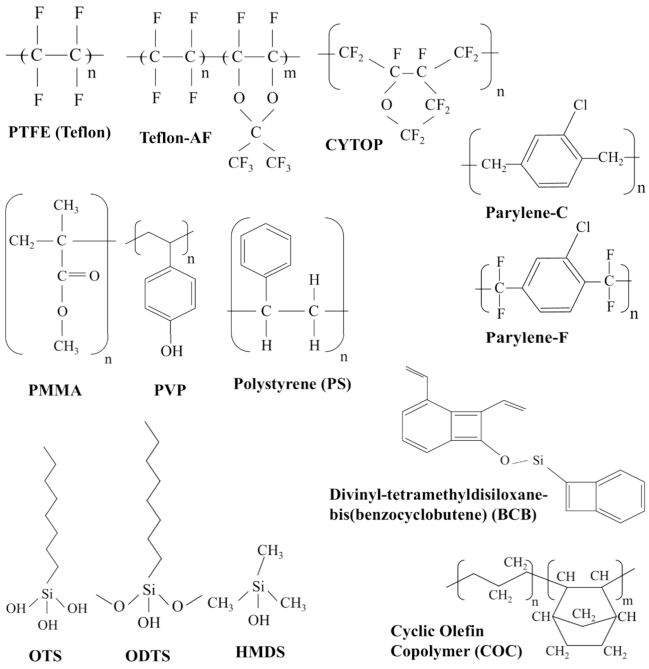

Figure 4. Chemical structures of common hydrophobic dielectric materials from Table 1.

Although Table 1 highlights relatively low dielectric constants for most hydrophobic gate insulators ($k \approx 2-4$), these materials continue to dominate solution-processed TFTs because their interface and manufacturing benefits outweigh the low capacitance. Their water-repellent, hydroxyl-free surfaces suppress deep trap formation, which minimizes hysteresis and enhances bias-stress stability.[59−61] In cases where high capacitance is required, they are used as a top layer in a bilayer structure with a high-k dielectric. These structures are discussed in subsequent subsections.

2.2. Inorganic High-*k* Dielectrics. Inorganic dielectrics such as SiO_2, hafnium oxide (HfO_x), and aluminum oxide (AlO_x) are popular inorganic high-k dielectric materials that have been used either as a single layer or in combination with other layers with hydrophobic surfaces. Inorganic high-k dielectric materials such as HfO_x, aluminum nitride (AlN), and bismuth niobate ($Bi_5Nb_3O_{15}$) with relatively hydrophobic surfaces have been used as gate dielectric in TFTs. These materials can exhibit moderately hydrophobic behavior when their surface energies are empirically verified to be lower than those of conventional oxides. This category is therefore applied only to oxides whose wettability has been characterized (e.g., water contact angle $\gtrsim 70°$ or surface energy $\lesssim 35$ mJ/m^2) and is not generalized to all forms of the material. The surface energy calculations (as low as 34.24 mJ/m^2) show that HfO_x naturally provides a favorable environment for organic semiconductor deposition, without requiring additional surface treatment.[62] AlN with a water contact angle of 72.9° leads to low-voltage operations (~5 V) in TFTs.[63] $Bi_5Nb_3O_{15}$ with a dielectric constant of 45 and a surface energy of 35.6 mJ/m^2, helps the pentacene layer with orthorhombic crystalline phase growth, providing better charge transport properties.[64]

2.3. High-*k* Inorganic Dielectrics and Low-*k* Hydrophobic Polymers. Bilayer dielectrics pair a thin, dense high-k oxide (e.g., Al_2O_3 or HfO_2) that supplies capacitance and blocks tunnelling with a hydrophobic, trap-free polymer top layer (CYTOP, Parylene, PVP, etc.). Polymers and inorganic dielectrics have different advantages in TFT applications, with polymers excelling in flexibility and low-cost processing, while high-k dielectrics (mainly metal oxides) deliver superior dielectric performance and stability. The inorganic bottom layer, such as HfO_2 or Al_2O_3, provides high dielectric constant and excellent leakage suppression due to its dense, insulating nature. Inorganic high-k dielectrics usually have hydrophilic surfaces. Meanwhile, the organic top layer, often composed of polymers like PVP or CYTOP, offers a smooth, hydrophobic, and trap-free surface that reduces interface trap density and charge trapping. This configuration also enhances environmental stability by blocking moisture and oxygen diffusion, improving long-term device reliability. Surface hydrophobicity is often achieved through surface treatments or by applying a suitable coating.[8,25,65−67] Figure 5 displays the histogram of

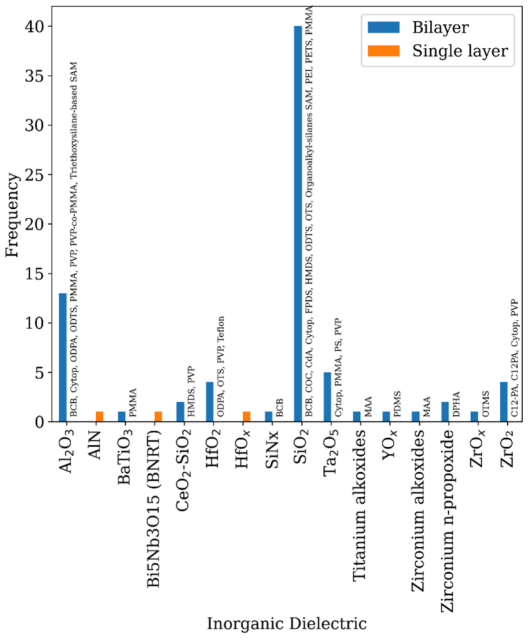

Figure 5. Histogram of literature references for inorganic dielectrics used in TFTs with a top hydrophobic surface (annotated with the name of materials they have been combined with).

literature references for various inorganic dielectric materials with hydrophobic surfaces used in TFTs, distinguishing between materials used in single layer and bilayer configurations. It shows the three inorganic dielectrics that have been used as a single layer and the rest as a bilayer structure.

SiO_2 has been used with different types of hydrophobic polymers such as spin-coated PVP (with a contact angle of 71.3°),[68] COC,[48] spin-coated CYTOP,[36,69] a few nanometer-thick Teflon layer,[26] vapor-phase deposited poly(1-vinylimidzole) (PVI) and inert poly(1H,1H,2H,2H-perfluorodecyl methacrylate) (pPFDMA),[70] trimethylsilyl-capped ladder-like polysilsesquioxane (LPSQ-TMS) which is functionalized with various organic side moieties such as methyl, n-propyl, phenyl, naphthyl, methacryloxypropyl (MA), and fluorooctyl,[71] and spin-coated hydroxyl-free polymers in general (PMMA, poly(α-methyl styrene) (PαMS), PVP, and poly(vinyl alcohol)

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(PVA)).[5] Hydrophobizing SiO_2 surface with HMDS improves the stability of the channel in both p-type and n-type organic field-effect transistors (OFETs).[72] The HMDS-treated OFETs show a reduction in bias stress effects, resulting in more stable transistor operation.[56] HMDS and PVP have been used to modify the high-k CeO_2−SiO_2 gate dielectric surface as well.[73] This modification reduces the number of hydroxyl groups (−OH) on the dielectric surface, which lead to better pentacene growth, and improved transistor performance. CYTOP and polystyrene (PS), significantly reduce the hysteresis in the transfer curves of the picene FETs, compared to HMDS-coated SiO_2 (all measurements were carried out under identical environmental and electrical conditions: gate voltage range = 0 to −120 V, preconditioned for 24 h at 10^{-6} Torr, then exposed to 8 or 10 Torr O_2). This results in improved device performance for O_2 gas sensing.[69]

The high-k dielectric tantalum pentoxide (Ta_2O_5) has also been used in bilayer structures with PVP, which results in an overall smooth and hydrophobic surface that improves the molecular structure in n-type and p-type semiconductors and reduces leakage current, providing a higher dielectric constant and better performance at lower operating voltages.[74,75]

Al_2O_3 too has been used with PVP,[76] HMDS,[6] and divinyltetramethyldisiloxane-bis(benzocyclobutene) (DVS-BCB) to ensure very low hysteresis (−5 V of gate source voltage, corresponding to quite high electric field of about 1.4 MV/cm (for 35 nm-thick pH1D6) applied as a constant voltage stress under inert N_2), improved mobility, and low operation voltage.[50] Three-layer systems of Al_2O_3, 3-glycidoxypropyltrimethoxysilane (GPTMS), and PMMA have also been used with cadmium sulfide (CdS) as an n-type inorganic semiconductor to produce TFTs with carrier mobility of 64.4 $cm^2/(V\ s)$.[7]

2.4. Hydrophobic SAM as the Top Layer. A SAM layer can be added to the surface of a dielectric to render it more hydrophobic. This means that most of the dielectric properties are those of the bulk dielectric layer and the SAM will modify the surface properties.[77,78] As depicted in Figure 6, when

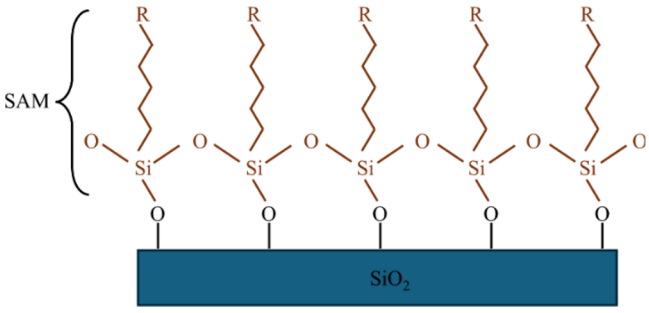

Figure 6. Schematic of the OTS SAM on the SiO_2 surface.

deposited on SiO_2, SAM molecules such as OTS and ODTS) form a monolayer on the surface due to chemical interactions between the silane groups of the SAM and the hydroxyl groups of the SiO_2 surface.[79] Another example is polyimide (PI) surface modified with octadecanethiol (ODT),[80] where ODT reacts with the unsaturated double bonds in the PI polymer. The carrier mobility in TFTs with ODT-treated PI dielectric is 0.41 $cm^2/(V\ s)$, compared to 0.11 $cm^2/(V\ s)$ for devices with untreated PI. This treatment increases the water contact angle from 67.3° to 87.7° and enhances the growth and adhesion of pentacene. Other examples are polysiloxane urethane acrylate composite (PSUAC) treated with ODTS,[79] OTS and ODTS treated SiO_2,[81,82] OTS treated HfO_2,[83] perfluorooctyltriethoxysilane (PETS) and phenyltriethoxysilane (PTS) treated SiO_2,[68] n-dodecylphosphonic acid (C12-PA) and n-octadecyltrimethoxysilane (OTMS) treated ZrO_x[84] and AlO_x coated with triethoxysilane-based SAMs.[85]

SAM treatment is in fact the most common method of increasing dielectric surface hydrophobicity due to its effectiveness and ease of deposition. This is reflected in Figure 7, which shows field effect mobility versus surface contact angle

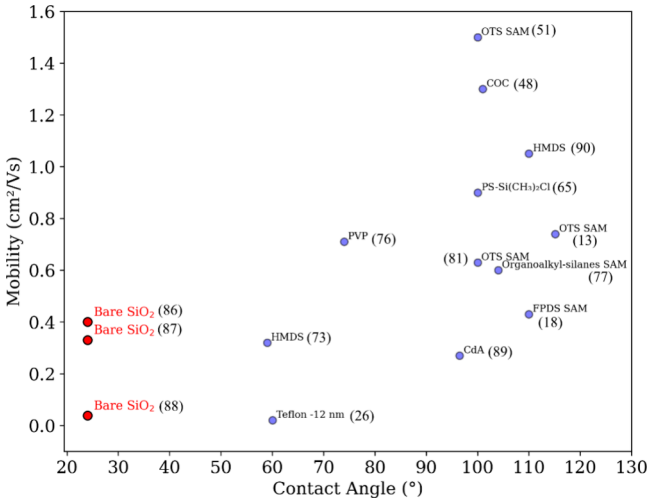

Figure 7. Hole mobility vs contact angles for SiO_2- and pentacene-based TFTs with different modifications to render the surface of the SiO_2 gate dielectric hydrophobic.

in SiO_2- and pentacene-based TFTs.[13,18,26,48,51,65,73,76,77,81,86−91] Higher mobility pertains to SAM modified surfaces with higher contact angle values.

3. TFT CONFIGURATIONS

The configuration of TFTs significantly impacts their electrical performance, stability, and the effectiveness of gate dielectrics, especially when using hydrophobic materials. Key configurations are bottom-gate bottom-contact (BGBC), bottom-gate top-contact (BGTC), top-gate bottom-contact (TGBC), and top-gate top-contact (TGTC). Figure 8 depicts these configurations. Each configuration offers advantages and challenges concerning charge injection efficiency, processing compatibility, and scalability for flexible electronics.

3.1. Bottom-Gate Bottom-Contact (BGBC). In the BGBC configuration, both the gate electrode and source/drain contacts are located beneath the semiconductor layer. This configuration offers excellent control over the gate electric field and allows for the use of a wide range of gate dielectrics, including high-*k* materials. It is often favored for its simplicity in fabrication and compatibility with solution processing. Hydrophobic dielectrics like CYTOP, Teflon-AF and PVP can be effectively incorporated in BGBC TFTs, improving the semiconductor/dielectric interface by reducing charge trapping and enhancing mobility.[3,67,68,92]

3.2. Bottom-Gate Top-Contact (BGTC). In the BGTC configuration, the gate electrode is beneath the semiconductor layer, while the source/drain contacts are deposited on top. This setup minimizes the damage to the gate dielectric during source/drain contact deposition, leading to lower contact

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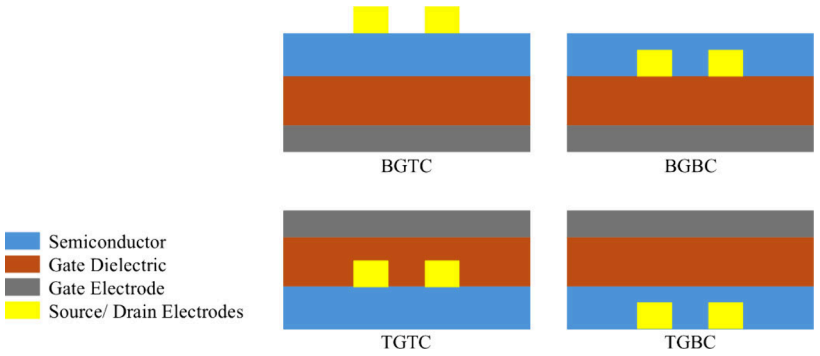

Figure 8. TFT stacked configurations.

resistance. The hydrophobic nature of dielectrics like PMMA, HMDS, and SAM treated dielectric surfaces in BGTC configurations helps improve the crystallinity of the semiconductor layer, resulting in better charge carrier mobility and reduced hysteresis.[4,46,55,77,83,93]

3.3. Top-Gate Bottom-Contact (TGBC). In the TGBC configuration, the source/drain contacts are located below the semiconductor layer, while the gate electrode and dielectric are deposited on top. In top-gate TFTs, hydrophobic dielectrics work like an encapsulation layer, minimizing environmental degradation and moisture absorption by the sensitive semiconductor layer. TGBC TFTs offer flexibility in choosing gate dielectrics and enable low-temperature processing, making them suitable for flexible electronics. Using materials such as poly(vinylidene fluoride-*co*-hexafluoropropylene) (P(VDF-HFP)), Merck's D series, and modified branched hydrocarbon with fluorine (MBHCa-F) series in TGBC TFTs enhances the dielectric/semiconductor interface, leading to improved stability and lower threshold voltage shifts.[94−96]

3.4. Top-Gate Top-Contact (TGTC). In TGTC configuration, both the gate electrode and source/drain contacts are located above the semiconductor layer. This means that the carriers are injected horizontally into the accumulation layer with minimal vertical transit. Despite reduced vertical transport, better encapsulation of the gate dielectric, and ease of alignment in lithography, there are difficulties in the deposition of the dielectric in the TGTC configuration. It might dissolve, swell or otherwise damage the underlying semiconductor film. Moreover, hydrophobic dielectrics have poor wetting behavior leading to nonuniform films or pinholes.[97−100]

Figure 9 shows the histogram of literature references using different TFT configurations incorporating hydrophobic dielectrics. Among more than 100 papers that were reviewed here (containing more than 130 different devices), only 9.5% were top-gate, and all of them were bottom-contact. In the vast majority of TFTs, including those using hydrophobic dielectrics, there is a noticeable preference for the bottom-gate configuration. This might be because of bottom-gate configurations being compatible with existing photolithography and thin-film deposition techniques.[49,101] Moreover, in bottom-gate configurations, the gate electrode and dielectric are deposited first, providing a uniform surface for the deposition of the subsequent layers. In addition, highly doped silicon wafers can be used as the back gate, which removes the need for gate fabrication. A high-quality SiO_2 dielectric can easily be grown and wafers with thermally grown SiO_2 are commercially available.

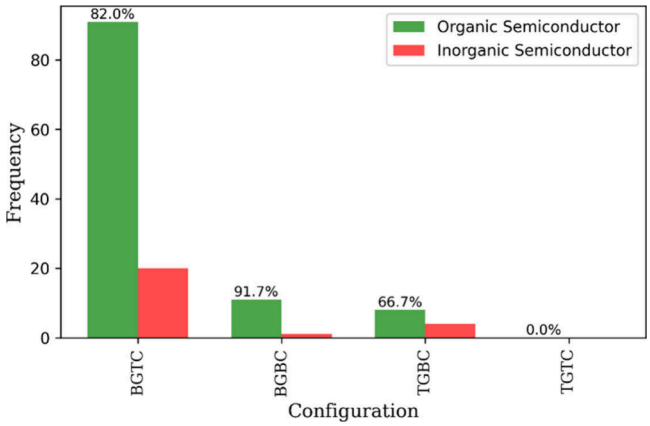

Figure 9. Histogram of literature references (109 studies) with different TFT configurations for organic and inorganic semiconductors using a hydrophobic dielectric.

Bottom contact configuration is particularly suited for inorganic TFTs because it aligns well with the standard photolithographic patterning techniques used in mass production. In this context, the inorganic nature of the semiconductor layers allows for robust fabrication without concerns such as charge injection barriers or mechanical damage during processing. For materials like indium gallium zinc oxide (IGZO), the bottom contact setup is preferred due to the ease of achieving uniform thin films over large areas with existing industrial techniques.[102] Figure 10 illustrates mobility and threshold voltage (V_{th}) trends across different TFT configurations for p-type and n-type semiconductors. BGTC configuration shows consistently higher mobility compared to other configurations. Threshold voltage spans a wide negative range across configurations, with BGTC showing more stable and less negative values. A combination of factors, such as semiconductor and dielectric material type affects the preference for BGTC and higher mobility values. Therefore, Figure 10 provides some insight into the statistical distribution of the TFTs based on configuration, but not much more beyond that.

4. THEORIES AND CHARACTERIZATION

This section explores the theoretical principles underlying hydrophobic gate dielectrics and outlines the experimental methodologies used to evaluate their properties. Several methods are employed to characterize hydrophobic gate dielectrics and their impact on TFT performance: gate bias stress, capacitance−voltage ($C-V$), surface energy and

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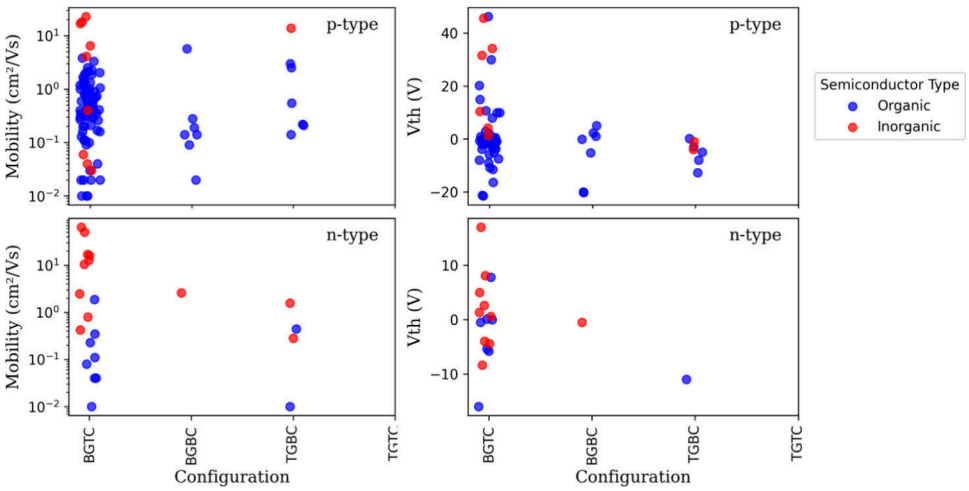

Figure 10. Mobility (log-scale) and threshold voltage versus configuration type for p-type and n-type, organic and inorganic semiconductors (extracted from 109 studies).

wettability, surface roughness, leakage current, and breakdown voltage. Finally, several devices fabricated with and without hydrophobic dielectrics are presented along with their performance metrics as evidence for device improvement as a result of using hydrophobic dielectrics or surface treatments.

4.1. Gate Bias Stress. Bias-stress tests are used to evaluate the stability and performance of transistors. Bias-stress test method typically involves the following steps and considerations:[70,103]

1. Initial characterization (pre-stress measurement): The transistor's baseline electrical characteristics is measured before applying any bias.
2. Applying the gate (and possibly drain) bias stress: A constant DC voltage is applied on the gate. In many tests, the drain may either be grounded or set to a small constant bias. Often, these tests are performed in controlled ambient or at different temperatures, to distinguish environmental effects from intrinsic device behavior.
3. Periodic or post-stress characterization: During or after a specific stress time interval, the bias stress is stopped, and the device's transfer curve is measured again. Therefore, changes in threshold voltage, drain current, subthreshold swing (SS), and other parameters are recorded.
4. Monitoring hysteresis and charge trapping: Hysteresis arises when slow traps or mobile ions in the dielectric (or at interfaces) cause the transfer curve to differ depending on the sweep direction. If the stress amplifies such effects, there will be a larger mismatch between the forward and reverse gate sweeps.

Specifically, bias-stress tests aim to investigate charge trapping at the semiconductor-dielectric interface. Hysteresis in the transfer characteristics of the transistor can also result from slow traps or mobile ions in the dielectric. These effects are worsened by bias stress and show ongoing problems in the device.[69] Fluorinated cross-linked PVP (F-cPVP) dielectric significantly reduces ΔV_{th} from 1.31 to 0.31 V under sustained stress (after 1-h gate stress at −3 V) compared to standard cPVP. These results prove the direct relationship between hydrophobicity and stability over time.[31] A hydrophobic capping layer (PMMA) on top of a polar dielectric (PVA, PVP, PS) and a layer of Al_2O_3 as the bottom dielectric layer, stabilizes device performance, reducing hysteresis (done in two controlled atmospheres: high vacuum ($\sim 10^{-4}$ mbar) and ambient air at 40−100 % RH (most data at 70 % RH)) and operational degradation over time.[104] The fluorinated polymer polypentafluorostyrene (PFS) has been combined with a more hydrophilic cross-linked polymer, poly(melamine-*co*-formaldehyde) acrylate, (PMFA) to form gate dielectric layer in pentacene-based OFETs. As the PFS content in the PMFA/PFS blend increases, the threshold-voltage shift under prolonged negative gate bias stress decreases dramatically. In devices made with pure PMFA (0% PFS), the threshold voltage shifts by over 1 V after three hours of stress; but for devices with 10% PFS in the blend, the shift is only about 0.2 V over the same period. Fluorinated polymers such as PFS are highly hydrophobic and chemically inert, so they introduce fewer deep trap states at the interface between the semiconductor (pentacene) and the gate dielectric.[105] OFETs incorporating COC-modified SiO_2 gate dielectrics exhibit enhanced bias stability, with ΔV_{th} under two hours of applied bias stress reduced from 10 V (for unmodified SiO_2) to under 2 V (under constant gate bias stress of −3 V, in a nitrogen (N_2)-filled glovebox). This shift, typically caused by the trapping of mobile carriers, is effectively minimized by the COC layer, which suppresses charge trapping both at the semiconductor−dielectric interface and within the organic semiconductor itself.[48]

Electrical hysteresis is also strongly affected by how the transfer curve is measured. Wider gate-voltage windows, slower sweep rates, and larger step widths allow slow traps more time to respond, inflating both ΔV_{th} and current lag. Conversely, narrower windows, faster sweeps, and finer steps suppress the apparent hysteresis. Therefore, it would be more accurate to report measurement protocols alongside material details when comparing device stability.[106]

4.2. Capacitance−Voltage (C−V) Measurements. The *C*− technique is widely used to extract information about the dielectric properties such as interface trap density, and charge storage in a device, particularly in metal−insulator-semiconductor (MIS) capacitors and OFETs.[71] The smoothness of the dielectric layer, the alignment of energy levels, and the ability of the dielectric to avoid trapping carriers all affect

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carrier mobility, threshold voltage, and stability.[47,47,107,107,108,108,108]

Standard $C-V$ measurements involve applying a small AC signal superimposed on a DC sweep of the gate voltage. By tracking the resulting current, one derives the capacitance at each bias point.[109] This method is typically conducted over a range of frequencies (e.g., kHz to MHz), and comparing the data reveals how quickly charges and interface traps respond to the applied field.[110]

Quasi-static $C-V$, by contrast, uses a very slow voltage sweep so that the device can nearly reach equilibrium at each step. This makes it especially sensitive to deep or slow traps that might be missed under faster AC conditions. By integrating the charging current over time, quasi-static measurements yield a more complete picture of the total charge stored in the semiconductor−dielectric system.[22] Together, standard AC and quasi-static $C-V$ methods help researchers distinguish different trap states, ion migration, and other mechanisms that affect device stability and performance.

In dielectrics prone to moisture uptake, water molecules and associated ions can migrate or reorient slowly under an applied electric field, contributing to the total polarization at low frequencies but not at high frequencies. This results in dispersion, which means the dielectric constant and thus capacitance is frequency dependent. At high frequencies (kHz−MHz), the slow-to-respond water-related polarization is negligible, leading to a smaller measured capacitance. At low frequencies or under quasi-static conditions, those slow dipoles and ionic charges have time to align or move, producing a larger effective capacitance. Such dispersion is a hallmark of moisture or other slow-polarization elements within the dielectric or at the interface. Hydrophobic dielectrics significantly reduce these moisture-related effects by minimizing water absorption at the dielectric−semiconductor interface. The fewer water molecules present, the fewer slow-moving or slowly reorienting dipoles exist to contribute at low frequencies. Consequently, the $C-V$ curves for hydrophobic dielectrics show less dispersion across a wide frequency range.[47,111,112]

$C-V$ measurements have also been conducted to evaluate the dielectric properties of a PVP/Al_2O_3 bilayer dielectric used in low-voltage OTFTs.[111] The contact angle measurements confirmed that PVP/Al_2O_3 is significantly more hydrophobic (water contact angle 70°) than bare Al_2O_3 (36°). The results showed less charge trapping compared to bare Al_2O_3 and improved transistor performance, including higher mobility and lower SS. The more hydrophobic nature of the gate dielectric results in reduced charge injection and storage effects, and a low leakage current density of 4.1 nA/cm^2 at 1 MV/cm. $C-V$ measurements showed stable capacitance across frequencies in P123−PS polymer blend-based OTFTs (see Figure 11), which is crucial for reliable OTFT operation. $J-E$ curves, which are plots of current density versus electric field (E), are tools to examine how a dielectric material conducts current under increasing electric field. It is a direct way to analyze how an insulator transitions from a high-resistance state to a regime where substantial current flows. The stability of the capacitance across different frequencies confirms that the hydrophobic dielectric does not suffer from ion migration or moisture-induced polarization.[47]

4.3. Surface Energy and Wettability. Surface energy and wettability play a vital role in determining the interfacial behavior of hydrophobic gate dielectrics in TFTs. These properties influence charge trapping, film formation, and overall device performance.

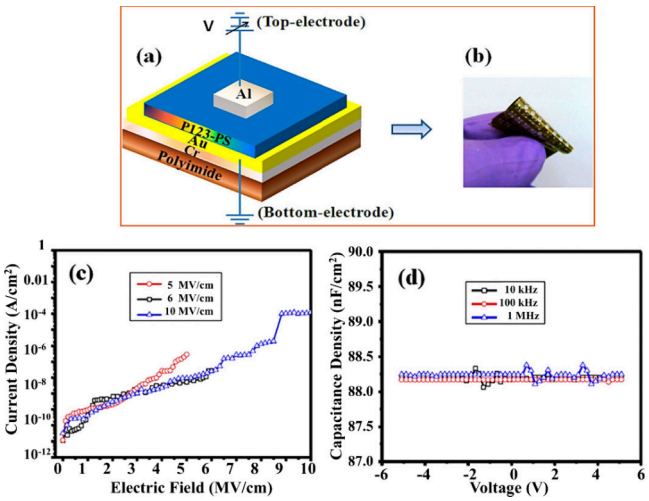

Figure 11. (a) Schematic of the P123−PS blend thin-film-based metal−insulator−metal (MIM) capacitor; (b) photograph of a flexible MIM capacitor on a 5 cm^2 flexible PI substrate showing the sample bent by hand; (c) $J-E$ and (d) $C-V$ plots for MIM device fabricated using P123−PS blend as a gate insulator. Reproduced with permission from ref 47. Copyright 2012 American Chemical Society.

4.3.1. Contact Angle Measurements: Assessing Wettability. Contact angle measurements are the standard technique for evaluating surface wettability. They quantify the angle formed between a liquid droplet and the surface to be evaluated. The measured value represents a static equilibrium condition that depends on how the droplet is formed and allowed to relax on the surface. Several methods are used for determining this equilibrium contact angle:

1. Sessile drop method: The most common approach is the sessile drop technique, where a droplet of known volume is gently placed on the sample surface. The droplet is allowed to equilibrate under ambient conditions, after which the tangent angle between the drop perimeter and the surface is measured (see Figure 12b−e).
2. Wilhelmy plate method: The Wilhelmy plate technique measures contact angle by immersing (and withdrawing) a thin plate of the substrate into the liquid of interest. The force balance on the plate is used to deduce the contact angle, eliminating some challenges of droplet shape and placement. This method is particularly useful for measuring dynamic contact angles (advancing and receding), though it can also capture an equilibrium value after motion stops.[113]
3. Capillary rise method: A third approach is to measure the height to which a liquid rises (or is depressed) in a capillary tube containing the substrate material. By relating the rise (or depression) height to known fluid properties and tube dimensions, one can calculate the contact angle. This method is often employed for porous or fibrous substrates and is well-suited to assessing average wettability characteristics over a large area.[114]

When interpreting static contact angles, a few subtleties must be considered, gravity effects, surface roughness, and hysteresis. For large droplets, the shape can be distorted by gravity, leading to a measured contact angle that is not strictly the same as the intrinsic angle determined solely by surface

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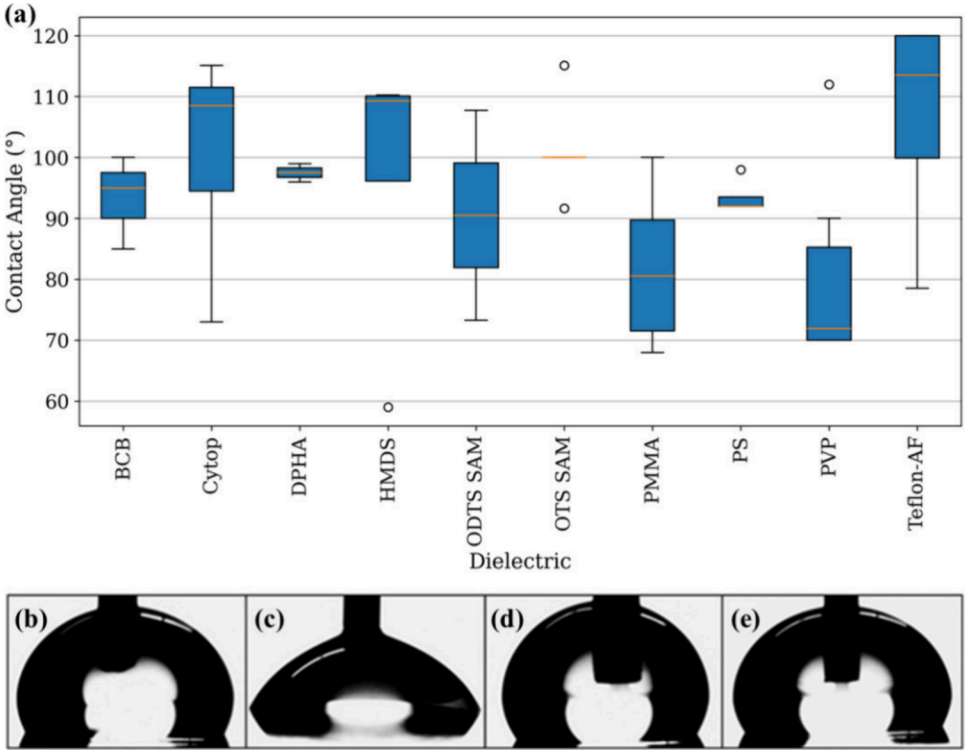

Figure 12. (a) Contact angle data for the 10 most frequently used top layer dielectric surfaces. Images of droplets on plasma-treated Teflon-AF films are shown in (b) for advancing and (c) receding mode. Similarly, droplets on nontreated films are shown in (d) for advancing and (e) receding mode. (b) to (e) Reproduced with permission from ref 3. Copyright 2022 Elsevier.

tension. Typically, measurement protocols use droplet volumes small enough (approximately 2−5 μL) that gravitational distortion is minimized. However, if larger droplets are required (e.g., for high-viscosity liquids or large surface areas), image-processing software must carefully fit the droplet's profile to account for gravitational sagging. Additionally, real surfaces are rarely perfectly smooth or compositionally uniform. Roughness can amplify both hydrophobicity (leading to larger observed angles if air pockets are trapped beneath the droplet) and hydrophilicity (if the liquid penetrates into surface asperities). Contact angle hysteresis (the difference between advancing and receding angles) can be substantial on rough or heterogeneous surfaces. Although this section focuses on static equilibrium angles, acknowledging hysteresis is critical. The true equilibrium angle often lies between the advancing and receding extremes.[115,116]

Figure 12a shows contact angle data for the 10 materials most frequently used as the top layer of dielectric surfaces. Figure 12b and c show images of droplets on plasma-treated (wettable) Teflon-AF films for advancing and receding modes, respectively. Similarly, in Figure 12d and e, droplets on nontreated (hydrophobic) Teflon-AF films are shown for advancing and receding modes, respectively. More hydrophobic surfaces often exhibit lower contact angle hysteresis.

The ideal dielectric must satisfy the requirements in terms of surface energy and at the same time exhibit strong enough adhesion to form a robust interface with the semiconductor. This means that its surface energy should match that of the semiconductor. For instance, a blend of PVP and poly(methyl silsesquioxane) (pMSSQ) as gate dielectric showed absence of hysteresis and excellent stability over time when compared with Teflon-AF. Despite having a lower water contact angle (100° to 117°), but still hydrophobic, PVP/pMSSQ provided the desired adhesion to single-walled carbon nanotubes (SWCNTs) deposited on top.[42]

4.3.2. The OWRK Method: Calculating Surface Energy. The Owens, Wendt, Rabel, and Kaelble (OWRK) method provides a quantitative approach to calculating surface energy by decomposing it into dispersive (van der Waals) and polar (dipole−dipole or hydrogen bonding) components.[64] This method is widely used for characterizing hydrophobic dielectrics, such as SAM-modified surfaces, where wettability influences film formation and charge transport.[61] To apply the OWRK method, first, contact angles are measured using two or more test liquids with known surface energies. Then through the following equation the dispersive and polar components of the surface energy can be calculated:

$$(1 + \cos\theta)\cdot\gamma_l = 2\left(\sqrt{\gamma_s^d\cdot\gamma_l^d} + \sqrt{\gamma_s^p\cdot\gamma_l^p}\right) \quad (1)$$

where θ is the contact angle, γ_l is surface energy of the liquid, γ_s^d is the dispersive energy of the solid, and γ_s^p is the polar energy of the solid.

The OWRK method has been used to characterize the surface energy of the SAM-modified dielectrics,[61] and AlN.[63] This method helps to understand how the hydrophobic and hydrophilic properties of surfaces impact the wetting behavior and subsequent film formation of organic semiconductors. It has also been used to investigate the surface energy modification in poly(vinyl acetate) (PVAc)-based dielectric layers in organic transistors.[108] Changing the ratio of dispersive and polar components alters hydrophobicity. With OTS treatment, the polar energy component becomes close to zero (0.04 mJ/m^2), leading to strong moisture resistance.

4.4. Surface Roughness. Surface roughness is a critical parameter in the performance of TFTs, particularly in devices

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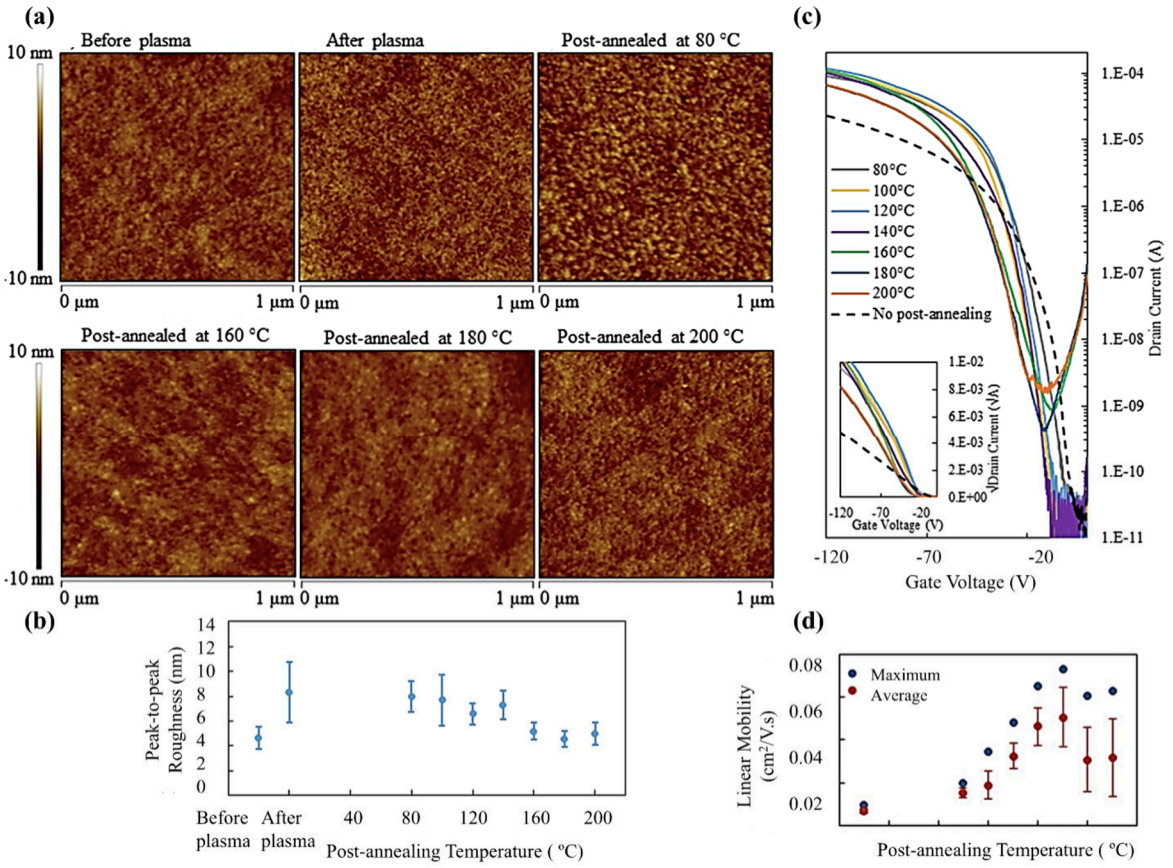

Figure 13. (a) AFM images of the Teflon-AF films before plasma, after plasma, and post-annealed at 80, 160, 180, and 200 °C. (b) Peak-to-peak roughness of Teflon-AF films before and after plasma treatment and after postannealing. (c) Transfer characteristics (I_dV_g) at V_d = 120 V for 20 μm channel length devices without and with different post-annealing temperatures. Inset shows the square root of drain current versus post-annealing temperature. (d) Linear field-effect mobility versus post-annealing temperature. Reproduced with permission from ref 3. Copyright 2022 Elsevier.

with hydrophobic gate dielectrics. Surface roughness encompasses multiple sources of variation: topographical irregularities, deposition conditions, chemical processes, substrate cleanliness, and can manifest at different length scales. In TFT applications, roughness may arise from both intrinsic factors such as the inherent microstructure of the material, and extrinsic factors such as contaminants or processing methods.[3,25,117] Measuring and quantifying roughness commonly involves a variety of techniques, each sensitive to slightly different aspects of a surface:

- Atomic force microscopy (AFM) provides high-resolution height maps from which statistical parameters (e.g., average roughness, root-mean-square roughness) and spatial correlations can be derived.[3,47,110]
- Contact profilometry or stylus profilometry physically traverses the surface with a probe; useful for larger-scale roughness measurements but less sensitive to nanometer-scale features.[73,108,118]
- Optical methods (e.g., white light interferometry): Noncontact approaches that can measure micrometer-scale variations across relatively large areas.[44,56,119−121]

Each technique highlights a specific roughness characteristic like short-range (nanoscale) vs long-range (microscale) variations. Consequently, surface roughness includes a spectrum of measurable properties, such as amplitude (height) parameters, lateral correlation lengths (the characteristic distance over which surface features repeat), and more sophisticated descriptors like fractal dimension. Accounting for these nuances is critical when correlating roughness to performance in TFTs, because different types and scales of roughness can have distinct impacts on charge transport, molecular packing, and interface stability.[34,63] In TFTs, smoother dielectric surfaces enhance the alignment and grain size of organic semiconductors, leading to reduced charge trapping and improved carrier mobility. Conversely, rough surfaces can disrupt the semiconductor's molecular ordering, increase trap density, and degrade electrical properties.[110,3,25,110] Furthermore, roughness can significantly impact leakage current. Localized thinning or uneven film deposition can increase conduction pathways leading to higher leakage, and, in hydrophobic dielectrics, can modify the contact angle due to the enhanced water-repelling properties that arise from increased surface texture.[6,107] Our previous study on Teflon-AF gate dielectrics offer valuable information on the influence of surface roughness and its reversibility as one of the factors on device performance.[3] Plasma treatment increases the roughness of Teflon-AF surface. The peak-to-peak roughness increases from 4.61 to 8.28 nm (see Figure 13). This increase in roughness disrupts the formation of uniform organic semiconductor films, deteriorating charge transport at the dielectric/semiconductor interface. Post-annealing, however, reduces surface roughness, which enhances charge transport and increases field-effect mobility.

4.5. Leakage Current and Breakdown Voltage Measurements. Leakage current is a critical parameter for

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assessing the insulating quality of gate dielectrics. Low leakage current indicates strong insulating properties, necessary for minimizing power loss, large I_{on}/I_{off} ratio, and ensuring device stability. Leakage current is typically measured by applying a known bias across the dielectric and recording the resulting current. It can be measured and recorded as the gate-source current (I_{gs}) at the same time with drain-source current (I_{ds}) measurement. The hydrophobicity of the dielectric layer can further reduce leakage by repelling moisture, which can otherwise degrade insulation through ionic conduction pathways.[31,47] Higher contact angle values can lead to lower leakage current (see Table 2). For example, the hydrophobic blend of a triblock copolymer and polystyrene (P123−PS) with a water contact angle of 92° exhibits lower leakage current density (~10^{-10} A/cm^2) compared to a traditional dielectric such as PVP,[90] leading to better transistor performance.[47] Another example is OTMS SAM treated ZrO_x with a contact angle of 105° and a leakage current of 4.5 × 10^{-7} A at 1 MV/cm,[122] while a more wettable C12PA SAM treatment with the contact angle of 101.60° leads to a slightly higher leakage current of 1.0 × 10^{-6}.[78] Similarly, F-cPVP with a fluorinated surface and a much higher contact angle than PVP (115° versus 70°) lowers the leakage current from 1.2 × 10^{-5} A to 1 × 10^{-7} A.[22]

Table 2. Different Combinations of Dielectric Structures with Their Effective Dielectric Constant, Contact Angle and Leakage Current Values (from Lowest to Highest)

Gate Dielectric	Effective Dielectric Constant	Contact Angle (°)	Leakage Current (A/cm^2 at 1 MV/cm)	Ref.
CYTOP	2.1	112.00	6.50 × 10^{-11}	34
P123 + PS	2.7	92.00	1.00 × 10^{-10}	47
PS-block-PMMA	3.1	82.80	7.46 × 10^{-10}	123
PSUAC	3.3	107.00	1.00 × 10^{-9}	79
SiO_2 + OTS SAM	2.95	100.00	1.00 × 10^{-9}	50
SiO_2 + ODTS SAM	2.95	107.71	1.00 × 10^{-9}	96
Hybrimer	3.8	80.00	4.10 × 10^{-9}	110
HfO_2 + PVP	12.1	73.30	1.20 × 10^{-8}	66
Methacryl-grafted hybrimer (MD)	4.2	80.00	1.50 × 10^{-8}	124
SiO_2 + dimethylchlorosilane-terminated polystyrene (PS-Si$(CH_3)_2$Cl)	3.2	100.00	1.00 × 10^{-7}	31
F-cPVP	3.2	115.00	1.00 × 10^{-7}	22
ZrO_x + OTMS SAM	12	105.00	4.50 × 10^{-7}	122
ZrO_2 + C12PA SAM	12	101.60	1.00 × 10^{-6}	78
Polyhedral oligomeric silsesquioxane (POSS)	3	90.00	1.50 × 10^{-6}	107
PVP	4.2	70.00	1.20 × 10^{-5}	90

Dielectric breakdown voltage testing evaluates a gate dielectric's ability to withstand high electric fields before transitioning from an insulating to a conducting state. Typically, this measurement involves ramping the applied voltage across an MIM or transistor structure while monitoring the current. In many cases, an abrupt increase in current clearly signals dielectric failure. However, some dielectrics can fail more gradually, as defects and pathways form over time, leading to progressively higher leakage currents. Additionally, real-world data often exhibits a statistical distribution of breakdown fields, with a subset of devices exhibiting lower-than-expected breakdown voltages due to manufacturing defects or intrinsic material inhomogeneities.[125,126]

Recent research underscores the versatility of hydrophobic dielectrics and their breakdown performance in TFTs. For example, hydrophobic plasma-polymerized PTFE/HfO_x-based hybrid dielectrics combine high mechanical durability with favorable leakage characteristics.[25] Carboxyl-containing hydrophobic polymeric dielectrics offer excellent electrical stability and high-k values for low-voltage printed transistor applications.[119] Meanwhile, reported organic−inorganic hybrids (hybrimers) that can be solution-deposited exhibit good insulating behavior, smooth surfaces, and low leakage currents.[110] Each of these approaches highlights how balancing breakdown voltage, dielectric constant, and surface properties is crucial to achieving both a robust performance and manufacturing feasibility in modern TFTs. Achieving a high dielectric breakdown voltage, therefore, remains critical for stable device operation. It ensures that the dielectric layer can tolerate the voltages required for switching without risk of catastrophic failure or excessive leakage. Figure 14 shows current density and breakdown voltage measurements along with the resulting capacitance or dielectric constant for the above-mentioned examples.

To visualize how candidate hydrophobic dielectrics navigate the competing demands of high permittivity, low surface energy and minimal leakage, we converted the data of Table 2 into the Ashby maps shown in Figure 15. The largest circles identify materials that best balance high dielectric constant, high contact angle and low leakage. Fluoropolymers such as CYTOP and F-cPVP dominate the upper-right, confirming that very low permeability to water vapor correlates with leakage currents below 10^{-10} A/cm^2 even at 1 MV/cm, albeit at the expense of the dielectric constant (Figure 15a). Bilayers ZrO_2 + C12PA SAM and ZrO_x + OTMS SAM combine $k \approx 12$ with sub-10^{-7} A/cm^2 leakage, underlining the value of a high-k oxide capped by an alkyl-phosphonate or silane SAM (Figure 15b). The negative correlation is evident: raising the dielectric constant generally lowers contact angle unless a hydrophobic capping layer is present. MD and PSUAC occupy a useful middle ground ($k \approx 4$, contact angle ≈ 80−90°) (Figure 15c).

The large circles in all panels highlight materials that approach a holistic optimum. They achieve high k with acceptable levels of leakage and surface energy. Conversely, PVP and PS-based dielectrics score well on k but appear as smaller circles because their leakage currents are an order of magnitude higher than those of SAM-capped oxides. These Ashby maps therefore provide an at-a-glance guide for selecting gate dielectrics that meet a specific design window, e.g., low operation voltage (high k) versus extreme bias-stress stability (low leakage and high contact angle).

4.6. Effect of Gate Dielectric Hydrophobicity on TFT Device Performance. Here, we present key studies that directly link water-repellent interfaces to lower trap densities, higher carrier mobilities, and tighter threshold-voltage control in TFTs. By comparing devices fabricated with and without hydrophobic dielectrics and tracking metrics such as field-effect mobility (μ_{fet}), SS, and V_{th}, these reports provide concrete, side-by-side evidence that the interface chemistry drives the observed performance gains.

Examples in Table 3 provide evidence of the effectiveness of hydrophobic surface treatments in TFTs. Hydrophobic surface treatments whether by phenyl-rich PVP on AlO_x, fluorinated

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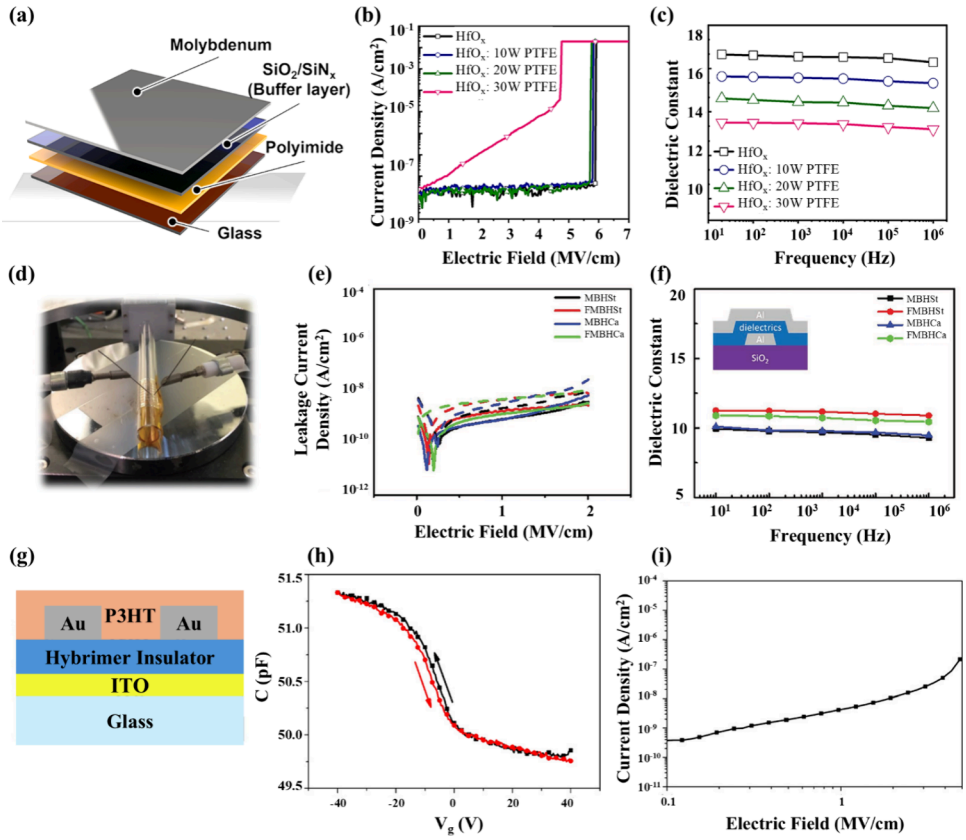

Figure 14. (a) Fabrication process of Plasma-polymerized hafnium oxide hybrid (PPH-hybrid) dielectric films. (b) $J-E$ curves of HfO_x and PPH-hybrid dielectric films with varying RF powers for PTFE deposition. (c) Dielectric constant of HfO_x and PPH-hybrid dielectric films vs frequency with varying RF powers for PTFE deposition. Reproduced with permission from ref 25. Copyright 2022 American Chemical Society. (d) Photo of leakage current measurement setup with bending stress, (e) leakage current density with flexible MIM devices (solid and dotted lines indicate pristine and bending case, respectively) (f) dielectric constant versus frequency plot and schematic image of the MIM device. Reproduced with permission from ref 119. Copyright 2021 Wiley Online Library. (g) The schematic transistor structure with a hybrimer gate dielectric. (h) $C-V$ hysteresis behavior of hybrimer gate insulator in MIS structure. RR-P3HT was drop cast on the hybrimer gate insulator. (i) Leakage current density of hybrimer thin film for the MIM structure. Reproduced with permission from ref 110. Copyright 2007 Elsevier.

MBH-based polymers, silazanes on SiO_2, COC overlayers, or PTFE-co-sputtering with HfO_x, replace polar −OH/C−O sites with nonpolar alkyl, phenyl or C−F groups.[48] Contact-angle and surface-energy measurements confirm this masking, while XPS, FTIR and $C-V$ analyses show that the now-inert interfaces bind far fewer H_2O/O_2 molecules and present markedly lower trap densities (e.g., 3.35×10^{12} to 2.87×10^{12} cm^{-2} eV^{-1} after fluorination).[110] With impurities eliminated, AFM and XRD reveal that small-molecule semiconductors nucleate in larger, more ordered grains; for pentacene on AlO_x/PVP or COC-coated SiO_2, grain enlargement accompanies mobility jumps from ~0.2 cm^2 V^{-1} s^{-1} to 0.55−1.3 cm^2 V^{-1} s^{-1}, subthreshold slopes sharpen toward the thermal limit.[48,119] The negative shift in threshold voltage indicates that the COC layer both introduces a small negative interfacial dipole and reduces water-related traps, allowing the device to turn on at a lower (more negative) gate bias. In general, when a hydrophobic layer (e.g., CYTOP, PS, PMMA) is applied, it passivates the surface hydroxyl groups (e.g., on SiO_2 surface) and reduces trap density, allowing for easier hole accumulation.[5,18,48]

These interfacial improvements cascade into the device and system-level gains: I_{on}/I_{off} ratios rise by one-to-3 orders of magnitude (e.g., 1.4×10^4 to 5.0×10^5 for AlO_x/PVP; 1×10^5 to 8×10^5 for SiO_2/COC),[119,48] bias-stress stability improves because fewer carriers are trapped during prolonged gating, and smoother semiconductor beneath the source−drain contacts reduces contact resistance from hundreds to single-digit kΩ·cm (SiO_2 vs FPDS-treated SiO_2).[18]

In short, rendering the dielectric hydrophobic suppresses chemical and morphological sources of disorder at the interface, allowing the intrinsic transport properties of the organic semiconductor to dominate and delivering faster, more stable, low-voltage OFET operation.[119]

5. DEPOSITION METHODS FOR HYDROPHOBIC GATE DIELECTRICS

Dielectric deposition methods in TFTs include solution-based methods,[127] vapor deposition methods, and self-assembly by immersion in SAM solution, each offering unique advantages. Vapor deposition methods like thermal, electron-beam evaporation and sputtering create uniform films for organic and inorganic dielectrics under vacuum conditions. Spin-coating and self-assembly methods such as SAM formation are simple and low-cost. Advanced printing methods like inkjet and gravure can be used for patterns and large areas. Specialized techniques such as ion gels and surface chemisorption are suitable for flexible and stretchable electronics. Figure 16 demonstrates deposition methods for

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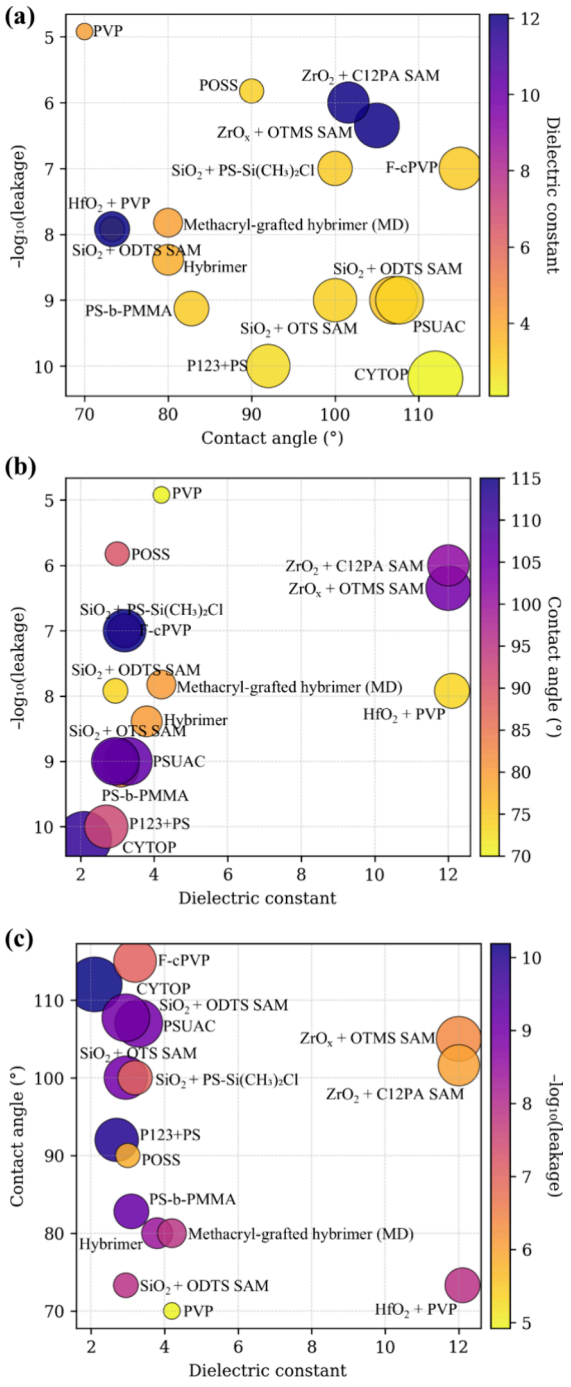

Figure 15. Ashby-style maps of hydrophobic gate-dielectric performance: (a) Contact angle (hydrophobicity) versus −log(leakage current at 1 MV/cm). Marker color encodes the dielectric constant. (b) Dielectric constant versus −log(leakage). Color encodes contact angle. (c) Dielectric constant versus contact angle. Color encodes −log(leakage). The largest circles identify materials that best balance high dielectric constant, high contact angle and low leakage.

the 10 most used hydrophobic dielectric materials in the last 20 years, with spin-coating being the most popular.

5.1. Challenges in Solution-Processed and Printed Electronics. Solution-processed and printed electronics offer advantages in cost, scalability, and flexibility. But, integrating hydrophobic dielectrics into these processes presents several challenges. Maintaining uniformity across large areas is difficult. Additionally, the inherently low surface energy of hydrophobic dielectrics complicates the deposition of subsequent layers. Overcoming these challenges requires careful tuning of surface properties, deposition conditions, and material combinations to enable stable, high-performance solution-processed TFTs. The low surface energy intrinsic to hydrophobic materials, while beneficial for environmental stability, complicates both the deposition process itself and the integration of other solution-processed layers, such as organic semiconductors or printed electrodes.[3,12,55,92,95,128]

5.1.1. Fabrication of Hydrophobic Gate Dielectrics. For solution-processable hydrophobic dielectrics, achieving uniformity, adhesion, and film stability is difficult. In spin-coating, dip-coating, and printing, maintaining consistent thickness across large areas is challenging. For example, high-viscosity polymers may form thicker edge regions.[129] The choice of deposition method affects film quality and scalability, with spin-coating being the most widely used for hydrophobic dielectrics in TFTs. However, polymer-based hydrophobic dielectrics can suffer from solvent interactions that lead to swelling or dissolution, as seen with poly(vinylidene fluoride-*co*-trifluoroethylene) (P(VDF-TrFE)) and PVP layers.[130] Additionally, batch-to-batch variations in polymer properties introduce reproducibility challenges, complicating large-scale manufacturing.[70] Precise control over deposition conditions and surface properties ensure stable electrical performance and scalability. Moderate O_2 plasma pre-treatment (5−8 s, 5 W) evens out spin-coated CYTOP but must be followed by a mild bake so the surface can "re-heal", otherwise carrier mobility drops.[92] Protein adsorption has been shown to raise CYTOP's surface energy just enough for uniform semiconductor casting while leaving leakage and trap density essentially unchanged.[12] For example, adding <0.5 wt % silica nanoparticles to TIPS-pentacene solution anchors the drying front and suppresses dewetting on PMSQ dielectrics.[48]

5.1.2. Fabrication of Other Device Layers on Top of Hydrophobic Dielectrics. Hydrophobic dielectrics, by design, repel aqueous and polar solvents, making it difficult to deposit solution-based materials like semiconductors, metal contacts, or interlayers on top.[3,43,44,131] For instance, gravure printing requires surfaces with optimized hydrophobicity for reliable transistor fabrication. However, excessive hydrophobicity can be problematic, leading to poor adhesion of gate electrodes and semiconductor layers. Surface energy adjustments (via surface treatments or tailored ink formulations) are essential to enable consistent film formation and reliable device performance.[95] The successful implementation of solution-processable hydrophobic dielectrics requires a balance between hydrophobicity and solution compatibility. By tuning surface properties,[43,132] using methods such as orthogonal solvents for subsequent layers,[133] temporary surface treatments,[3] tuning stage temperature during electrode deposition,[44] and employing hybrid structures,[21] it is possible to achieve high-performance TFTs with stable operation and scalable manufacturing. In our study on Teflon-AF OTFTs, we fabricated 20 μm-channel OTFTs on Teflon-AF by combining a brief plasma step with inkjet Ag printing. The subsequent anneal reversed much of the plasma damage, restoring both hydrophobicity and charge carrier mobility.[3]

Moving from lab-scale prototypes to high-throughput manufacturing of TFTs on hydrophobic dielectrics requires harmonizing material properties and process conditions at an industrial scale. While bench-scale demonstrations often focus on proof-of-concept (e.g., spin-coating small samples),

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Table 3. TFT Examples of Using Hydrophobic Dielectrics with Characterization Evidence

Dielectric	Semiconductor	Contact Angle (deg)	μ_{fet} ($cm^2/V{\cdot}s$)	V_{th} (V)	SS (V/dec)	I_{on}/I_{off}	N_{trap} ($1/eV{\cdot}cm^2$)	Ref.
Bare AlO_x	Pentacene (p-type)	36	0.17	−3.2 (estimate)	0.7	1.4×10^4	Not reported	119
AlO_x/PVP		70	0.55	−5	0.5	5.0×10^5	Not reported	
MBHSt	C_{10}-DNTT (p-type)	74 (estimate)	0.25	−2.61	0.677	Not reported	3.39×10^{12}	110
FMBHSt		83 (estimate)	0.76	−5.05	0.582	Not reported	3.26×10^{12}	
MBHCa	C_{10}-DNTT (p-type)	71 (estimate)	0.28	−1.44	0.752	Not reported	3.35×10^{12}	110
FMBHCa		85 (estimate)	1.18	−4.26	0.548	Not reported	2.87×10^{12}	
Untreated SiO_2	Pentacene (p-type)	77.0	0.25	−7.08	Not reported	10^6	Not reported	18
HMDS-treated SiO_2		85.9	0.42	−11.7	Not reported	10^6	Not reported	
FPDS-treated SiO_2		89.0	0.43	−10.8	Not reported	10^6	Not reported	
HfO_x	IGZO (n-type)	39.27	13.21	1.3	0.35	2.83×10^8	2.99×10^{12}	25
HfO_x:PTFE 10 W		51.51	15.28	1.5	0.35	2.82×10^8	2.82×10^{12}	
HfO_x:PTFE 20 W		78.56	16.04	0.64	0.32	1.83×10^9	2.34×10^{12}	
HfO_x:PTFE 30 W		80.00	12.07	0.60	0.32	1.51×10^4	7.86×10^{12}	
SiO_2	Pentacene (p-type)	68	0.23	14 (estimate)	0.527	1×10^5	1.71×10^{12}	48
SiO_2/COC		101	1.3	5 (estimate)	0.234	8×10^5	5.6×10^{11}	
Untreated SiO_2	PTCDI-C8 (n-type)	50.3	0.13	Not reported	Not reported	1.7×10^5	Not reported	5
SiO_2/PαMS		98.0	0.33	15.01	Not reported	2.4×10^5	Not reported	
SiO_2/PVP		72.5	0.17	46.31	Not reported	4.0×10^4	Not reported	
SiO_2/PMMA		76.1	0.14	10.72	Not reported	4.8×10^5	Not reported	
SiO_2/PVA		21.0	0.056	20.22	Not reported	4.3×10^4	Not reported	

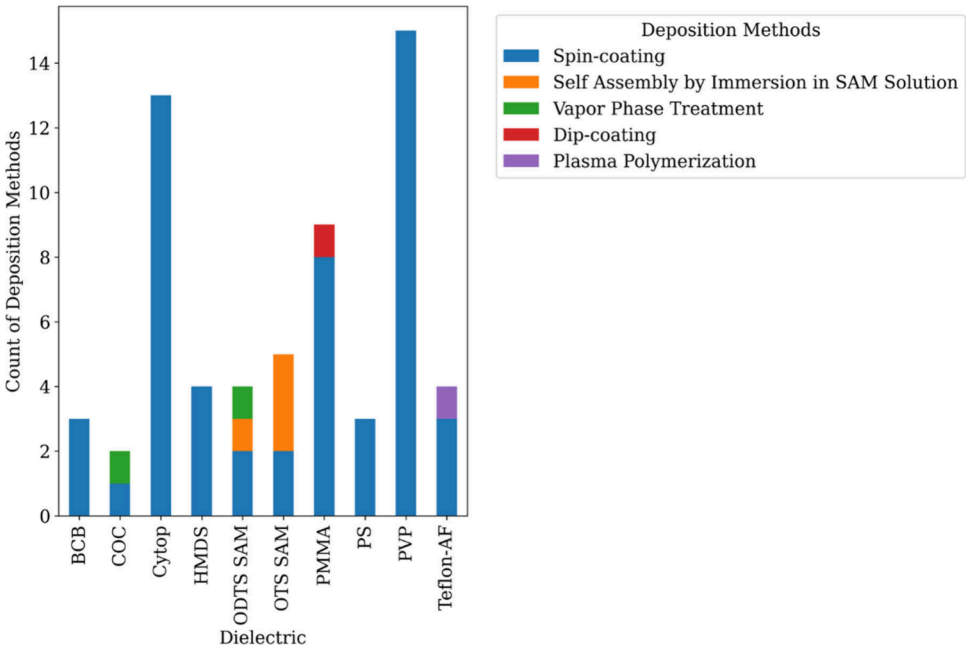

Figure 16. Deposition methods of the 10 most used hydrophobic dielectric materials in the TFT literature.

commercial production demands consistency, scalability, and cost-effectiveness. For example, maintaining the same molecular weight, cross-linker ratios, and solvent compositions from batch to batch is critical, so the hydrophobic surface remains uniform and reproducible.[134] Variations in polymer synthesis or solution rheology can undermine the ability to deposit subsequent layers reliably at scale.[119] In roll-to-roll or batch processes, real-time thickness and surface-energy monitoring (e.g., contact angle or optical inspection) allows early detection of deviations in hydrophobic film quality before thousands of devices are compromised. Manufacturers can thus fine-tune parameters (e.g., line speeds, temperature, dispensing rates) on the fly.[95] Large-area printing or coating methods (e.g., slot-die, inkjet, or gravure) must overcome the intrinsic low surface energy of hydrophobic substrates, which can cause beading or dewetting in overlayers. Dense and pinhole-free hybrid dielectrics can still be compatible with subsequent solution processes if solvent polarity, drop spacing, and temperature are precisely optimized.[110] Temporary surface treatments like plasma, ozone, or mild chemical priming may be systematically applied inline to adjust surface energy just enough for the next layer to wet uniformly, then revert (via thermal annealing) to the dielectric's original hydrophobic state. This approach can be integrated into standard manufacturing flows with minimal added complexity if well-controlled.[3] From an industrial standpoint, both thermal budget and coating speed are major cost drivers. Processes that require high-temperature curing or long dwell times can create bottlenecks. With PTFE/HfO_x

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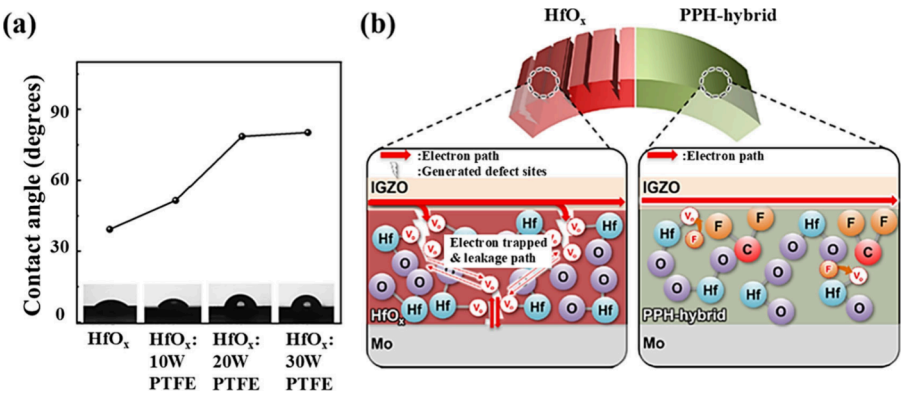

Figure 17. (a) Contact angle measurements of HfO_x and PPH-hybrid film. (b) Schematic illustration of the effects of repetitive bending stress on HfO_x and PPH-hybrid dielectric films. Reproduced with permission from ref 25. Copyright 2022 American Chemical Society.

hybrid dielectrics, a controlled plasma or sputtering approach can yield stable films suitable for downstream fabrication without prolonged annealing.[25]

In summary, while spin-coating remains the most widely used technique for laboratory-scale fabrication of hydrophobic dielectrics, its scalability and uniformity over large areas remain limited. Vapor-phase methods such as CVD offer superior uniformity and control, but at the expense of higher cost and potential incompatibility with flexible substrates. Printing techniques are attractive for scalability but require precise tuning of ink and surface properties to overcome dewetting and adhesion issues.[3,61] Hybrid approaches, such as combining a thin hydrophobic SAM with a thicker, high-*k* dielectric or using temporary surface treatments, currently show the most promise for balancing performance, processability, and scalability, but involve trade-offs in process complexity and device reliability.[135]

6. APPLICATIONS

Hydrophobic gate dielectrics have opened new possibilities in the development of advanced TFT technologies. In this section, we will explore the diverse applications where hydrophobic gate dielectrics can play a significant role.

6.1. Flexible Displays. Flexible displays are one of the most promising applications of hydrophobic gate dielectrics. The demand for bendable screens in smartphones, tablets, and wearable devices drives the need for TFTs that can operate reliably under mechanical stress. By utilizing hydrophobic dielectrics such as CYTOP, SAM- or HMDS-treated surfaces, TFTs show enhanced mechanical durability and flexibility,[23,47,73,95,136−139] as well as low operating voltages,[61,63,122,140] which are critical factors for the realization of flexible displays. Coating CeO_2−SiO_2 gate dielectric with PVP increases water contact angle from 11° to 74° and the surface energy decreases from 70.00 mJ/m^2 to 26.32 mJ/m^2, leading to large pentacene grains, reduced leakage current and improved device reliability. These characteristics enable the fabrication of TFTs with low operating voltages and high performance, ideal for flexible display applications.[73] AlO_x with SAM treatment results in high performance dielectric with excellent electrical insulation, making ZnO nanowire transistors suitable for OLED applications.[141] Another promising dielectric for low-voltage, flexible OTFTs is $Bi_5Nb_3O_{15}$, which is mechanically flexible and optically transparent. The pentacene-based TFTs have low operating voltage (−5 V), a high I_{on}/I_{off} ratio (10^5), and reliable bending performance (showing stability after 10^5 bending cycles).[64]

6.2. Bioelectronics and Implantable Devices. Bioelectronics including implantable medical devices require materials that are biocompatible, stable, and resistant to the body's internal environment. Wearable sensors are becoming increasingly popular for continuous health monitoring, and requiring lightweight, flexible, and durable electronics.[75−78] Hydrophobic dielectrics provide the necessary moisture resistance and stability to operate effectively in biological settings, as well as the potential for integration into soft and wearable electronics.[142] Pentacene-based strain sensors were built using a hybrid dielectric layer of PVP and Ta_2O_5, demonstrating excellent performance.[74,75] The hybrid PVP/Ta_2O_5 dielectric combines the high capacitance of Ta_2O_5 with the low leakage current and smooth surface of PVP. This leads to improved mobility of 1.89 cm^2/(V s), a low threshold voltage of −0.5 V, low-voltage operation (~4 V), and an I_{on}/I_{off} ratio of 10^3. The strain sensor can detect bending radii as small as 8 mm. This sensitivity is a result of the improved pentacene crystallinity and interface properties caused by the hydrophobic dielectric surface.[41] PPH-hybrid dielectric with high-*k* HfO_x dielectric combined with RF-sputtered PTFE, offers excellent flexibility, thermal stability, and hydrophobicity (see Figure 17). It maintains a low leakage current density (~10^{-8} A/cm^2) even after 10,000 bending cycles (2 mm radius), whereas HfO_x alone becomes leaky. For HfO_x-based IGZO TFTs, 10,000 tensile bending cycles lead to a drop in I_{on}/I_{off} (from 1.35 × 10^8 to 1.27 × 10^4), an increase in SS (from 0.35 to 1.04 V/dec), and higher off-current and interface charge density due to mechanical damage. In contrast, PPH-hybrid dielectric-based IGZO TFTs remain stable, with I_{on}/I_{off} changing only slightly (from 3.75 × 10^8 to 1.15 × 10^8) and SS (from 0.32 to 0.35 V/dec), demonstrating its superior mechanical robustness and flexibility[25] (see Table 4).

6.3. Environmental and Chemical Sensors. Hydrophobic gate dielectrics are also beneficial in chemical and environmental sensors, where maintaining sensitivity and stability under varying conditions is essential. These sensors often operate in humid environments, making hydrophobic properties necessary for consistent performance.[9,69,143] One example is ammonia (NH_3) sensing for environmental monitoring and diagnostic purposes. Using hydrophobic PMMA as the gate dielectric in OFETs leads to a structured organic semiconductor layer, achieving high sensitivity, fast

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Table 4. Comparison of Parameter Shifts in HfO_x and PPH-Hybrid Dielectric Based IGZO TFTs Caused by Various Mechanical Stresses[a]

Sample	Bending Stress	Mobility ($cm^2/V{\cdot}s$)	I_{on}/I_{off}	SS (V/dec)	V_{th} (V)
HfO_x-based TFT	Before bending	13.65	1.35×10^8	0.35	1.38
	After bending stress (10000 cycles)	5.07	1.27×10^4	1.04	2.38
PPH-hybrid-based TFT	Before bending	16.86	3.75×10^8	0.32	1.03
	After bending stress (10000 cycles)	16.99	1.15×10^8	0.35	0.96

[a]Reproduced with permission from ref 25. Copyright 2022 American Chemical Society.

response, and recovery for detecting low concentrations of ammonia (down to 100 ppb).[9] See Figure 18a–c.

6.4. Logic Gates. The application of hydrophobic gate dielectrics in logic gates is based on their impact on the performance and stability of TFTs. Hydrophobicity of the gate dielectric prevents moisture-induced degradation, which is especially useful for flexible logic circuits operating in ambient conditions. Hydrophobicity ensures long-term stability and reliability of the logic gates, even under bias-stress conditions.[42,141,144,145] The hydrophobic MBHCa-F dielectric layer reduces charge trapping at the dielectric/semiconductor interface, maintaining stable operation in OTFTs. These logic gates have been fabricated via electrohydrodynamic (EHD) jet printing, which allows for precise deposition of the hydrophobic dielectric.[144] The voltage transfer curves of the NOT gates show clear inverting properties with stable high and low logic levels across different supply voltages. See Figure 18d–f.

6.5. Memory Devices. Hydrophobic dielectrics are good candidates for floating gate nonvolatile memory applications, because they satisfy the requirements of low operational voltage, data retention and device stability.[53,146] The enhanced data retention comes from the low surface energy of hydrophobic dielectrics which minimizes charge leakage.[147] Adding fluorophenyl azide (FPA) cross-linker to polymeric dielectrics leads to phase separation, where hydrophobic functionalities move toward the surface while polar carboxyl groups are pushed into the bulk region. As a result, charge trapping sites such as hydroxyl (−OH) groups are eliminated. Therefore, the memory device exhibits higher charge retention, lower leakage current, and improved operational stability.[119] In another example, fluorinated polyimide (FPI) has been used with SiO_2 dielectric to improve the memory effect with a memory window of 25 V within 500 ms under a gate voltage of 100 V, and over 10,000 s data retention.[148] FPI has smooth surface topographies and surface energy values that make it suitable for use in bottom-gate organic transistors.[149] Poly(4-fluorostyrene) (FPS), a hydrophobic polymer, has been used as a gate dielectric in OFETs and nonvolatile memory devices. FPS has deep bulk traps which ensures stable charge storage with a memory window of 108 V, retention over one month in ambient air, and high carrier mobility of 11.2 $cm^2/V{\cdot}s$. At the same time, its hydrophobicity protected the device against moisture, improving environmental stability.[150]

Sometimes the desired outcome is achieved by using a triple-layer dielectric structure. For example, a triple layer of PVP/P(VDF-TrFE)/PVP with the top PVP layer being hydrophobic combines the benefits of high field-effect mobility, low leakage, and memory retention. While, the middle P(VDF-TrFE) layer is responsible for a large memory window and threshold voltage shifts.[130] Hydrophobic metal nanoparticles are also promising candidates for creating scalable, stable and high performance OFET memory devices. They have been employed in multilayer-stacked structures as charge-trapping elements in OFET memories with a memory window exceeding 145 V.[147] See Figure 18g and h.

7. FUTURE RESEARCH DIRECTIONS

Hydrophobic gate dielectrics show promise for improving TFT performance. Yet, many challenges remain. New materials, surface treatments, and device architectures must be explored.

More advanced hydrophobic dielectrics are needed to push device performance further. Current materials (e.g., CYTOP, HMDS, fluorinated polymers) work well but have limitations when used in solution-processed electronics. They can be incompatible with certain solvents or process steps, risking delamination and uniformity issues,[47] and they may degrade under mechanical wear or environmental stress, limiting long-term durability.[137] Their low dielectric constants can demand higher operational voltages and risk leakage or breakdown unless thicker films are used.[108] Many are insufficiently elastic, making them prone to cracking under bending or stretching.[151] Also, some may be toxic such as PTFE-based, perfluorinated materials and silane treatments, posing safety and environmental concerns with growing regulatory scrutiny and partial bans on certain fluorinated compounds.[152−154]

Combining high-k inorganic oxides (HfO_2, Al_2O_3) with hydrophobic polymers (PVP, PMMA) can boost both electrical performance and water repellency.[4,5,68] More of these combinations should be examined, while their compatibilities must be investigated and improved. Materials that repair microcracks on their own can improve durability in flexible electronics. For instance, triacetate cellulose (TAC) dielectric in OTFTs has shown strong mechanical stability. Devices maintained stable mobility and I_{on}/I_{off} ratio after 100 bending cycles. TAC's biodegradability and low gate leakage make it highly promising for green electronics.[5,137] TFTs need lower voltages for energy-efficient mobile devices. Further optimization is required for hydrophobic dielectrics. Pairing high-k dielectrics with hydrophobic low-k layers may enable operation below 1 V without losing performance. Flexible and stretchable devices require dielectrics that maintain properties under repeated bending. Highly elastic hydrophobic materials are essential for next-generation wearables. Moreover, materials that are both nontoxic and water-repellent could enable new medical implants and biosensors. Hydrophobic dielectrics mitigate moisture damage, but long-term outdoor and wearable application is still challenging. Combining hydrophobic dielectrics with advanced barriers can protect devices from humidity, UV light, and extreme temperatures.

Surface modifications such as SAM and silane treatments improve hydrophobicity and reduce charge traps, but more work is required to increase scalability. Large-area methods for SAMs (e.g., OTS, ODTS) and fluorinated coatings could be used in commercial products as well.

Better measurement methods will clarify how hydrophobic dielectrics behave at the molecular level. Additionally, fine-tuning capacitance−voltage tests such as optimizing the voltage sweep range, step size, and frequency, and temperature

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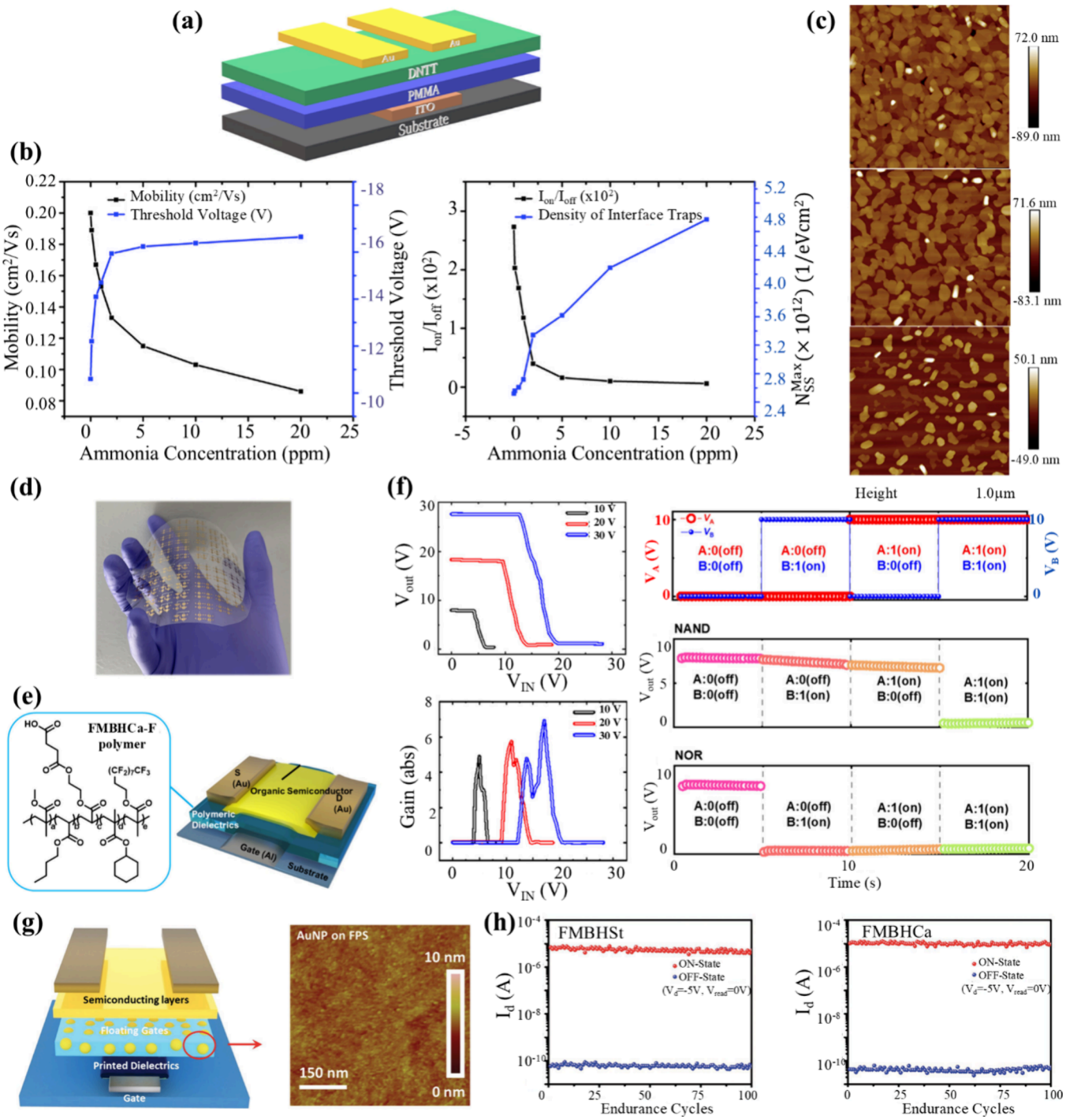

Figure 18. (a) The schematic structure of a bottom-gate, top contact DNTT-based OFET. (b) Variation of mobility, threshold voltage, I_{on}/I_{off} and number density of interface states of one device with respect to different NH_3 concentrations. (c) Atomic force microscopy images of DNTT on PMMA, from top to bottom: 50 nm thick film, 12 nm thick nanocrystalline porous film and, 5 nm thick discrete film. Reproduced with permission from ref 9. Copyright 2021 Elsevier. (d) Photograph of the flexible OTFT array with MBHCa-F-0.4 polymeric insulators. (e) Device schematics with MBHCa-F polymeric insulators (MBHCa-F-0.01, −0.06, −0.1, and −0.4). (f) VTC and voltage gain curve; (d) input and output curve of NAND and NOR gates; the unit OTFTs constituting all of the logic described in the figure were prepared with MBHCa-F-0.4 insulating film-based OTFTs. Reproduced with permission from ref 144. Copyright 2023 American Chemical Society. (g) Schematic illustration of floating gate memory devices with printed dielectrics and AFM image of AuNPs embedded cross-linked PS layer. (h) Dynamic switching behavior of memory devices with write-read-erase-read cycles. Reproduced with permission from ref 119. Copyright 2021 Wiley Online Library.

conditions can pinpoint trap densities and charge behavior in hydrophobic layers.

Hydrophobic dielectrics could benefit devices other than standard TFTs. For example, stable, low-power dielectrics can aid synaptic transistors for brain-like computing. Hydrophobic materials may improve piezoelectric or triboelectric generators for self-powered sensors. Moreover, they can also be used to enhance phototransistor and photovoltaic performance due to water-repellency and reducing moisture damage.

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8. CONCLUSIONS

Hydrophobic gate dielectrics have emerged as critical components in the advancement of TFT technology, offering significant improvements in device performance, stability, and longevity. By leveraging materials with low surface energy and enhanced moisture resistance, researchers have successfully addressed key challenges in TFTs, such as charge trapping, hysteresis, and bias stress. These advancements are particularly relevant for applications in flexible electronics, wearable sensors, bioelectronics, and environmentally robust devices, where device reliability and durability are paramount.

Despite these achievements, there remain substantial opportunities to further explore the potential of hydrophobic gate dielectrics. Innovative approaches, such as self-healing dielectrics, integration of hybrid bilayer structures, scalable SAM deposition techniques, and more in-depth characterization of the dielectric/semiconductor interface are ways to optimize device performance while benefiting from dielectric hydrophobicity. Furthermore, exploring new applications beyond conventional TFTs, such as neuromorphic computing and energy harvesting devices, could unlock the full potential of hydrophobic dielectrics in emerging technologies.

In conclusion, hydrophobic gate dielectrics represent a promising avenue for advancing next-generation electronics. By bridging the gap between fundamental materials science and practical device applications, these materials have the potential to redefine the landscape of flexible, low-power, and high-performance electronic devices. Continued research and development in this field will not only enhance the performance of existing technologies but also pave the way for new, innovative applications in the years to come.

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

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